

Programme Details

DAY 1

09:00 to 09:30

REGISTRATION

09:30 to 10:00

INAUGURATION

10:00 to 11:15 **Session 1:**

Best design practices for implementing today's multimillion gate count Complex System-on-Chip (SoC) in submicron technologies

Mr. Hemanshu Vernenker, *Sr. Staff Manager, Qualcomm.*

11:15 to 11:30

TEA

11:30 to 13:00 **Session 2:**

A practical look at SoC design from RTL to gds2 using Synopsys ICC platform

Mr. Prasan Shanbhag, *Sr. Applications Consultant, Synopsys.*

13:00 to 13:30

LUNCH

13:30 to 16:30 **HANDS ON 1:**

A **hand's on lab session** using Synopsys ICC platform. Attendees will go through various stages of physical implementation: synthesis (using DC compiler), place and route, floor planning, power planning, placement, clock tree synthesis, routing, (ICC), parasitic extraction (Starcc) and static timing analysis (Primetime)

Mr. Prasan Shanbhag, *Sr. Applications Consultant, Synopsys.*

DAY2

09:30 to 10:45 **Session 3:**

Challenges of ultra-low power design for next generation wireless devices

Mr. Prasan Shanbhag, *Sr. Applications Consultant, Synopsys.*

10:45 to 11:00

TEA

11:00 to 12:15 **Session 4:**

Power Analysis, Electromigration and IR Drop of multimillion gate SoCs using Apache Redhawk

Mr. Manjunath, *Consultant, Broadcom*

12:15 TO 13:15 **Session 5:**

System on Chip Verification challenges and methodologies

Mr. Bebeck Nobel, *Sr. Engineer, Nvidia*

13:15 TO 13:45

LUNCH

13:45 TO 14:15 **Session 6: PANEL DISCUSSION**

Opportunities for research projects and future collaboration between academia and industry in VLSI domains. The years ahead: a new era in SoC design - challenges of designing a System on a Chip in 20nm technology

– *Industry panel*

14:15 to 16:15 **HANDS ON 2:**

Continuation of Hands on 1.

16:15 to 16:45

VALEDICTORY

Patrons

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Dr. R Chenraj Jain, President - Jain University Trust

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Dr. K. Venkatesh, Director & CTO

Dr. T.G.S.Moorthy, Professor & Advisor

Mr. Hemanshu Vernenker, Qualcomm

Workshop Convenors :

Prof. K. Chandrasekhar, Programme Co-ordinator

Prof. K.T.Srirangaraj

Organising Committee:

Mr. Deepak V. Ingale

Mr. Jagadeesh B. C.

Mr. Bhanuprakash. N.

Venue :

Centre for Emerging Technologies™

Jain Knowledge Campus

9th Block, Jayanagara, Bengaluru

Reach us at:

9 4 8 0 4 2 8 3 0 9 - Prof. K. Chandrasekhar

9 3 4 1 2 8 5 3 4 1 - Prof. K.T.Srirangaraj

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A two day **WORKSHOP** on **ADVANCED TRENDS IN LOW-POWER SoC VLSI DESIGN**

on **October 5 & 6, 2012**



Organized by :



Centre for Emerging Technologies™

Jain University

Bengaluru



Indian Society for Technical Education

Karnataka



NGIT

Jayanagara, Bengaluru

JAIN UNIVERSITY

JAIN UNIVERSITY, a part of the Jain Group of Institutions (JGI), was established in 2009 with the objective of providing quality education and has since built a massive educational edifice in a record time of just under a decade. The inspiration behind this noble endeavor has been the need to provide quality and modern education as in the west, with strong Indian cultural values. Jain Group of Institutions is today a conglomerate of 28 educational institutions, all different from the other but working in unison towards the cherished goals of the group. The significant growth of these institutions has not been a chance occurrence. It is a commitment that stems from a need to create a good learning environment and encourage students to continuously engage in further learning not only in their chosen disciplines but also other related fields including sports and global tours.

CENTRE FOR EMERGING TECHNOLOGIES™

The "Centre for Emerging Technologies"™ established in 2008 at the Jain Global Campus amidst sylvan surroundings on a 300 acre campus under the aegis of Industry-Institute relationship program is a global hub for promoting the new technologies and undertaking Research and Consultancy in various domains of engineering. Towards this a platonic relationship is being built up with a number of companies and institutions alike wherein the academic community gets to associate and work on state-of-the-art technologies addressing different industry verticals. A qualified group has been set up to support the centre taking into account that the economies of the coming decade shall be knowledge based driven economies.

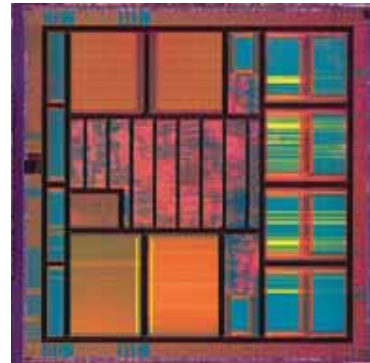


Academicians, students and professionals with cross cultural sensitivity, skills and a broad base of knowledge would be in significant demand in the coming decade, the need would be to empower them with such skills (required for academic activity and active research) so that they would be able to effectively contribute to the growth of new economies. The Centre for Emerging Technologies at Jain University addresses the same by promoting new and advanced technologies by establishing units of excellence jointly with industrial support in diverse domains of science and technology.

NGIT

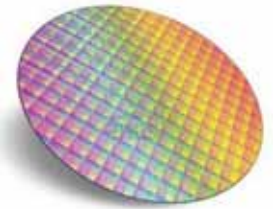
NGIT is the premiere VLSI institute in Bangalore founded by a group of passionate educationists and industry veterans to boost the educational ecosystem in India. NGIT provides world-class training in industry standard EDA tools and conducts industry relevant projects, courses and workshops. All faculty members at NGIT are in senior technical or management positions in leading semiconductor companies and bring to NGIT a formidable breadth and depth of technical expertise.

NGIT offers leading edge programs in VLSI and Embedded Systems ranging from RTL, verification, Design-For-Test, physical design, circuit design, and mixed signal design to DSP and Embedded Systems. Research is in NGIT's DNA, (its faculty members have published multiple patents and publications) and as a result, several publications have emerged from projects conducted by NGIT. For more information, please contact us at < contact.ngitworld@gmail.com >



About the workshop

The complexity of today's SoCs (System on chip) is staggering. How does a team of a few hundred engineers manage to deliver a chip with more than a billion transistors in less than a year with such amazing precision? What



are the design practices, tools and processes behind the scenes that have transformed the world of technology and computing around us? What are the some of the Herculean challenges that engineers have to face day in and day out to accomplish this feat? The 2012 VLSI workshop brought to you by CET, Jain University and NGIT gives you insights into the challenges of multimillion gate design, verification, physical implementation, timing sign off and manufacturing in an industry where engineers are single-minded about conforming to Moore's law even when all the odds seem stacked against them.

A special feature of the workshop is the hands-on lab session which will give the participants an intimate look at what it takes to design these low power complex SoCs using leading edge tools from Synopsys, Cadence and other EDA vendors.

In addition, the workshop addresses the challenges of tomorrow, such as – The obstacles that an engineer will face when designing SoCs at 20nm; The impact of double patterning technology on the various phases of the design cycle; The validity of Moore's law in the coming years; and more.

Lastly, there will be an interactive session with the faculty members to explore joint projects and research opportunities to foster further collaboration in the field of VLSI.

Target participants :

Faculty of Engineering Colleges *and*
Post-Graduate Students

Participants number is limited to 40